B

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE** #19

**Group Art Unit:** 2182

**Examiner:** Butler, D.

**Applicants:** Krishna Rangasayee et al.

**Serial No:** 08/707,694

**Filing Date:** September 4, 1996

**For:** PROGRAMMABLE LOGIC DEVICE HAVING AN INTEGRATED PHASE LOCK LOOP

---

## DRAWING TRANSMITTAL

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

In response to the Notice of Allowability mailed March 1, 2001 indicating that formal drawings are due, enclosed are three (3) sheets of formal drawings.

Respectfully submitted,

By: _____
Christopher P. Maiorana
Registration No. 42,829
CHRISTOPHER P. MAIORANA, P.C.
24025 Greater Mack, Suite 200
St. Clair Shores, Michigan 48080
(810) 498-0670

Date: April 11, 2001

**Attorney Docket No.:** 0325.00063

### CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via First Class Mail in an envelope with sufficient postage and is addressed to: Assistant Commissioner for Patents, Washington, DC 20231, on April 11, 2001.

By: Mary Donna Berkley
Mary Donna Berkley